Claims 1-13 and 16-20 were examined. The Examiner has objected to the Drawings for informalities. Applicants supply "replacement drawings" herewith which address those informalities.

Claims 1-13 and 16-20 have been newly rejected under 35 USC 102(b) as being anticipated by the teachings of the Dean patent. For the reasons set forth below, Applicants contend that the claims are patentable.

In response to the rejections under 35 USC 102(b) as anticipated by Dean, Applicants respectfully traverse the rejection. The Dean reference is directed to a system and method for estimating execution rates of program execution paths as a measure the operation of processors (Col. 5, lines 35-36). Under the Dean method, one or more program instructions to be profiled are randomly selected (Col. 5, line 43 and Col. 6, lines 35-38). During the execution of the randomly selected instructions, a "profile record" of what happens during execution is accumulated in a set of internal registers (Col. 5, lines 43-45). The information in the profile registers includes stage latencies, cache misses, memory addresses and targets, and results (Col. 5,

lines 52-59). The collected information is then analyzed to evaluate performance.

Applicants respectfully assert that the Dean patent does not teach or suggest the invention as claimed. The present invention provides a method and system to generate compressed memory reference traces which are ordered according to the program control flow for better compression and decompression. As taught and claimed, the present method, program storage device and apparatus perform the steps of selecting each sequence of events in a control flow for said program, obtaining a sequence of memory reference values for each of the events during execution of the program, and compressing the values to generate a compressed sequence of values for each event, which is a compressed memory reference trace.

Dean neither teaches nor suggests creating a memory reference trace, let alone generating a compressed memory reference trace during program execution. Rather, Dean expressly teaches that instructions are randomly selected for execution. As such, Dean clearly does not select each sequence of events in a control flow of the program as is expressly claimed. Where Dean gathers profile information on some random instructions, the present invention obtains a sequence of values for each of the sequence of events.

Further, the present invention compresses the sequence of values and collects a series of compressed sequences of values for events to generate a compressed memory reference trace. In contrast, Dean simply collects profiling data for random instructions and, when the instructions are retired or aborted, Dean analyzes the collected information in the profile registers.

Dean does not teach or suggest compressing the information and adding it to other compressed information to form a compressed memory trace. Finally, Dean does not teach or suggest ordering values of the compressed memory trace according to information in the control flow of the program in order to generate an uncompressed trace and storing the compressed and uncompressed traces.

Anticipation under 35 USC 102 is established only when a single prior art reference discloses each and every element of a claimed invention. See: In re Schreiber, 128 F. 3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997); In re Paulsen, 30 F. 3d 1475, 1478-1479, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994); In re Spada, 911 F. 2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990) and RCA Corp. v. Applied Digital Data Sys., Inc., 730 F. 2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). Since the Dean patent does not teach the claimed steps and means for creating a compressed

memory reference trace, it cannot be concluded that Dean anticipates the invention as claimed.

Based on the foregoing amendments and remarks, Applicants respectfully request entry of the amendments, reconsideration of the rejections, and issuance of the claims.

                              Respectfully submitted,
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